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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/019,437	12/31/2001	Yasuyuki Doi	60188-124	4255

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EXAMINER
NELSON, ALECIA DIANE

ART UNIT	PAPER NUMBER
2675	11

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DATE MAILED: 04/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/019,437	DOI ET AL.	
	Examiner	Art Unit	
	Alecia D. Nelson	2675	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9-14* is/are allowed.

6)☒ Claim(s) *1-5 and 15-17* is/are rejected.

7)☒ Claim(s) *6-8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 7.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 5/07/03 has been considered by the examiner. Also, references listed on the IDS submitted 12/03/01, which were indicated as not being considered by the examiner due to lack of a copy being provided, have been considered. The references include JP 5-35220, 5-273520, 5-94159, 7-191635, and 4-86787.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. ***Claim 1*** is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claim recites that the reference voltage wire unit is configured to supply at least one of the plurality of reference voltages to *each* of the source driver circuit devices, however the specification and drawing describe that only one of the source driver circuits are supplied with the reference voltages from the reference voltage wire unit, wherein in-chip reference voltage wires extending to the other end of the source driver for supplying a the reference voltages to the additional source drivers. Therefore the claimed subject matter is indefinite for failing to particularly point out and distinctly claim the subject matter.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. ***Claim 1*** rejected under 35 U.S.C. 103(a) as being unpatentable over Park (U.S. Patent Application Publication No. 2001/0043176).

With reference to the claim Park teaches a liquid crystal display device (1) using COG, including a upper glass substrate (10) and al lower glass substrate (12), column driving ICs (14), and row driving ICs (16), a electrical signal modulation circuit (18), which supplies signals required for these column driving ICs (14) and row driving ICs (16) (see paragraph 7). There is also taught a voltage signal wiring for producing voltage signals to be supplied to the drivers, a source wiring unit (GCW, CTW, CSW) capable of supplying signals to each of the source driver circuits.

While Park teaches that it is possible for the voltage signal wiring to be formed in the pad regions of the lower glass substrate, and is connected via the flexible cable to the electrical signal modulating circuit similar to the other wirings (see paragraph 8), which would make it obvious that the wiring would be separate from the source wiring unit being that they are all separated from one another, and that the voltage wires extend through an area (lower glass substrate (12)) on the liquid crystal panel, and an area on the source driver circuit devices.

Therefore it would have been obvious to one having ordinary skill in the art to allow for the source wiring unit and the reference voltage wiring unit to be separate from on another as suggested by Park in a device similar to that which taught by Park which allows for a liquid crystal display driving circuitry which allow the reference voltage wires to extend through an area on the liquid crystal panel in order to thereby simplifying the circuit configuration and/or the wiring structure of the liquid crystal display device and thereby minimizing the size of the liquid crystal display device.

7. ***Claims 2, 15, and 16 are*** rejected under 35 U.S.C. 103(a) as being unpatentable over Park as applied to **claim 1** above, and further in view of Sasaki et al. (U.S. Patent No. 6,221,849) and Applicant's admittance of prior art.

With reference to **claims 2, 15, and 16**, Parks fails to teach the usage of in-chip reference voltage wires or the usage of at least two branch reference voltage wires.

Sasaki et al. teaches that the driving circuit (1) includes a plurality of in-chip reference voltage wires (10) extending from one end to the other end of the source

driver circuit for supplying a plurality of reference voltages different from one another (see Figure 3). Sasaki et al. also teaches that various power voltages are input to the driver (1) via the power input (11) and supplied to circuit components such as the buffer amplifiers (4, 8) and other circuitry and are output to the next driver IC (see column 7, lines 6-15)

The admitted prior art teaches the usage of two branch reference voltage wires (131) branching off from a corresponding in-chip reference voltage wire of the plurality of in-chip reference voltage wires, and a selection circuit (134) for selecting a voltage for driving the liquid crystal element (see Figure 10).

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow for the usage of the branch reference voltage wires and a selection circuit as disclosed by the admitted prior art in the driver circuits which allow for in-chip wiring as taught by Sasaki in the display device similar to that which is taught by Parks in order to thereby reduce the required wiring area for signal transmission in order to produce higher resolution for larger screen sizes without increasing the dimensions of the frame region of the display.

8. ***Claims 3, 4, and 17*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Sasaki et al. in view of the admitted prior art.

With reference to **claims 3 and 17**, Sasaki et al. teaches a semiconductor integrated circuit device provided in a liquid crystal module and carrying thereon a source driver circuit (23) for driving a liquid crystal element wherein the source driver

includes a plurality of in-chip reference voltage wires (10) extending from one end to the other end of the source driver circuit for supplying a plurality of reference voltages different from one another (see Figure 3). Sasaki et al. also teaches that various power voltages are input to the driver (1) via the power input (11) and supplied to circuit components such as the buffer amplifiers (4, 8) and other circuitry and are output to the next driver IC (see column 7, lines 6-15)

The admitted prior art teaches the usage of two branch reference voltage wires (131) branching off from a corresponding in-chip reference voltage wire of the plurality of in-chip reference voltage wires, and a selection circuit (134) for selecting a voltage for driving the liquid crystal element (see Figure 10).

Therefore it would have been obvious to one having ordinary skill in the art to allow for the usage of the branch reference voltage wires and the selection circuit as disclosed by the admitted prior art in the driver circuits similar to that, which is taught by Sasaki et al. to thereby reduce the required wiring area for signal transmission in order to produce higher resolution for larger screen sizes without increasing the dimensions of the frame region of the display.

9. With reference to **claim 4**, Sasaki et al. fails to teach that the semiconductor integrated circuit device further includes a subdivided voltage production circuit wherein the selection circuit selects on of the subdivided voltages.

The admitted prior art teaches the limitations of claim 4, including the subdivided voltage production circuit (132) and the selection circuit (134) (see pages 5-6).

Therefore it would have been obvious to on having ordinary skill in the art to allow the device of Sasaki et al. to include the subdivided voltage production circuit and the selection circuit as taught by admitted prior art in order to generate voltage signals for controlling the brightness of light passing through the liquid crystal element when driving the liquid crystal display panel thereby producing higher resolution for larger screen sizes without increasing the dimensions of the frame region.

10. ***Claim 5*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Sasaki et al. and admitted prior art as applied to **claim 1** above, and further in view of JP Patent No. 3-165118, hereinafter 3-165118).

Sasaki et al. and the admitted prior art teaches all that is required as explained above with reference to **claim 1**, however fail to teach that the buffer has an offset canceling function.

3-165118 teaches the usage of two switched capacitor circuits for a complementary operation, which are capable of canceling an offset voltage of an input terminal and an output terminal (see page 1).

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow for a buffer which is disclosed in 3-165118, in a device similar to that which is taught by Sasaki et al. and the admitted prior art in order to cancel an offset voltage between the input terminal and the output terminal in order to reduce noise generated and thereby improving the resolution of the display device.

Response to Arguments

11. Applicant's arguments with respect to ***claims 1-14*** have been considered but are moot in view of the new ground(s) of rejection.

Further section IV-Prior Art Rejections does not pertain to the rejection applied to the claims and therefore has not been considered as part of the response.

Conclusion

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alecia D. Nelson whose telephone number is (703) 305-0143. The examiner can normally be reached on Monday-Friday 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steve Saras can be reached on (703) 305-9720. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

14. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

adn/ADN
April 17, 2004

Anne Hirsch Nelson
4-17-2004